Process Variation and Radiation-Immune Single Ended 6T SRAM Cell

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***Abstract*— The leakage power can dominate the system power dissipation and determine the battery life in battery-operated applications with low duty cycles, such as the wireless sensors, cellular phones, PDAs or pacemakers. Driven by the need of ultra-low power applications, this paper presents single ended 6T SRAM (static random access memory) cell which is also radiation hardened due to maximum use of PMOS transistors. Due to process imperfection, starting from the 65 nm technology node, device scaling no longer delivers the power gains. Since then the supply voltage has remained almost constant and improvement in dynamic power has stagnated, while the leakage currents have continued to increase. Therefore, power reduction is the major area of concern in today's circuit with minimum-geometry devices such as nanoscale memories. The proposed design in this paper saves dynamic write power more than 50%. It also offers 29.7% improvement in T_{WA} (write access time), 38.5% improvement in W_{PWR} (write power), 69.6% improvement in W_{EDP} (write energy delay product), 26.3% improvement in W_{EDP} variability, 5.6% improvement in R_{PWR} (read power) at the cost of 22.5% penalty in SNM (static noise margin) at nominal voltage of V_{DD} = 1 V. The tighter spread in write EDP implies its robustness against process and temperature variations. Monte Carlo simulation measurements validate the design at 32 nm technology node.**

***Index Terms*— Random dopant fluctuation (RDF), line edge roughness (LER), read access time, static random access memory (SRAM), drain induced barrier lowering (DIBL), short channel effect (SCE)**

I. INTRODUCTION

Due to aggressive scaling, fluctuations in device parameters are more pronounced in minimum-geometry devices commonly used in area-constraint circuits such as SRAM (static random access memory) cells [1]. SRAM is a highly used circuit of modern chips. SRAM constitutes more than half of chip area and more than half of the number of devices in modern designs [2]. As per ITRS prediction, embedded cache will occupy 90% of an SoC (system-on-chip) by 2013 [3]. Even today, an H-264 encoder for a high-definition television requires, at least, a 500 kb memory as a search-window buffer that contributes 40% to its total power dissipation [4]. The SNM (static noise margin) model in [5] assumes identical device threshold voltages across all cell transistors, making it unsuitable for predicting the effects of threshold voltage mismatch between adjacent transistors within a cell. Therefore, designer will require reinvestigation and analysis of SNM in scaled technologies to ensure stability of SRAM cell.

Low power operation is a feature that has become a necessity in today's SoCs and μPs (microprocessors); hence, power consumption of SRAM modules must be reduced and has been under extensive investigation in the technical literature [6]. However, with the aggressive scaling in technology, substantial problems are encountered when the conventional 6T (six transistors) SRAM cell architecture is utilized. Therefore, extensive research is carried on designing SRAM cells for low power operation in the deep sub-micron/nanometer regimes [7−9]. The common approach to meet the objective of low power design is to add more transistors to the original 6T cell. An 8T cell can be found in [7]; this cell employs two more transistors to access the read bitline. Two additional transistors (thus yielding a 10T cell design) are employed in [8], [9] to reduce the leakage current. However, these approaches increase the cell area and thus not suitable for area constraint cache design.

The objective of this paper is to propose a new SRAM cell that is scalable to small feature sizes such as 32 nm. The novelty of this cell is that its design requires only 6 transistors (6T). The architecture of the cell is different from that of conventional 6T SRAM cell which is differential in nature whereas the proposed cell is single ended. Moreover, the design utilizes mostly PMOS transistors to make it radiation-hardened. The simulation results of the proposed single ended PFET-based 6T SRAM cell (hereafter called SEP-6T) are compared with differential 6T SRAM cell (hereafter called Dif-6T) and it is demonstrated that the proposed scheme offers significant advantages in terms of write dynamic power, write access time, write power, write EDP and read power at the expense of static noise margin. Moreover, simulation results using HSPICE confirm that the proposed SEP-6T is suitable for implementation at 32 nm CMOS technology.

The remainder of the paper is organized as follows. Various failure mechanisms are briefly reviewed in Section II. Section III briefly discusses impact of scaling – DIBL (Drain-Induced Barrier Lowering) and SCE (Short-Channel Effect), read stability, and write-ability. Section IV presents brief discussion on read/write operation, cell sizing and dynamic power saving of proposed SEP-6T. Section V explains the simulation measurement results and compares proposed design with Dif-6T. Finally, Section VI concludes the paper.

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II. FAIURE MECHANISMS IN SRAM

Failures in SRAM cell may be of three types – hard failures, soft failures and parametric failures. 1) *Hard failures* are caused by open or short. 2) *Soft failures* – there are major three sources of soft failures. They are alpha particles released from the radioactive impurities such as packaging materials, high energy neutrons from terrestrial cosmic radiations and the interaction of cosmic ray thermal neutron. 3) *Parametric failures* – since these failures are caused by the variations in the device parameters, these are known as the parametric failures. Parametric failures include access failure defined as unacceptable increase in SRAM cell access time; read failure is defined as flipping of cell content while reading; write failure is defined as inability to write to a cell and hold failure is defined as flipping of the cell state in the standby mode, especially when V_{DD} approaches or falls below DRV (data retention voltage) [10−13].

III. IMPACT OF SCALING AND READ/WRITE STABILITY

Due to scaling, substantial problems arises while designing conventional 6T SRAM cell. Therefore, impact of scaling on read stability and write-ability is required to be reinvestigated at scaled technology such as 32 nm technology node.

A. DIBL and SCE on Scaled Devices

It is well known, that the threshold voltage is given by

$$V_t = V_{t0} + \gamma\left(\sqrt{(2\,|\,\phi_F\,|+V_{SB})} - \sqrt{2\,|\,\phi_F\,|}\right) \qquad (1)$$

where V_{t0} is the threshold voltage at V_{SB} = 0 V and is mostly a function of the manufacturing process, difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc; V_{SB} is the source-bulk voltage; $\phi_F = V_T \ln(N_A/n_i)$ is the bulk Fermi potential (where V_T = kT/q = 26 mV at 300 K is the thermal voltage, N_A is the doping concentration of acceptor ion of substrate, n_i is the intrinsic carrier concentration in pure silicon); $\gamma = \sqrt{(2qN_A\varepsilon_{si})}/C_{ox}$ is the body-effect coefficient (where ε_{si} is the permittivity of silicon, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance).

Equation (1) is suitable for estimating the threshold voltage for long channel devices (> 1 μm). It fails to model threshold voltage of nanoscaled devices. To model threshold voltage for nanoscaled devices many factors such as SCE (short-channel effect), RSCE (reverse short-channel effect), NWE (narrow-width effect), DIBL (Drain Induced Barrier Lowering) effect, etc., are to be taken into account. In short-channel devices, the depletion region around the drain increases as V_{DS} increases and it extends into the channel region. Conceptually, the drain voltage assists the gate voltage in the depletion process. Hence, V_t decreases due to DIBL

TABLE I.
DIBL EFFECT ON THRESHOLD VOLTAGE

V_{DS}	Vt	η_{DIBL}
0	0.6292	Indeterminate
0.1	0.6101	0.191
0.2	0.5910	0.191
0.3	0.5719	0.191
0.4	0.5528	0.191
0.5	0.5337	0.191
0.6	0.5146	0.191
0.7	0.4954	0.191
0.8	0.4763	0.191
0.9	0.4572	0.191
1.0	0.4381	0.191

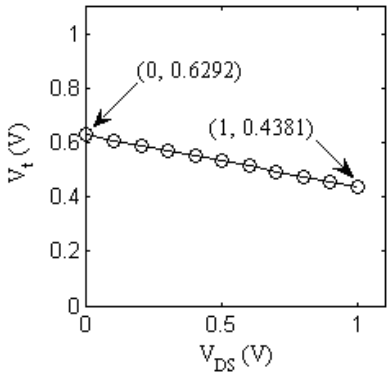

Figure 1. Threshold voltage (V_t) versus drain to source voltage (V_{DS}) of NMOS transistor at 32 nm technology node. V_t variation due DIBL

effect. The DIBL effect can be modeled as

$$V_t = V_{t0} - \eta_{DIBL} V_{DS} \qquad (2)$$

where V_{t0} is the threshold voltage at V_{DS} = 0V, and η_{DIBL} is the DIBL coefficient approximately equal to 0.191 for NFET. This is computed and verified by simulation using BPTM 32 nm technology. The results are tabulated and plotted in Table I and Fig. 1 respectively, which shows dependency of V_t on V_{DS}. The Fig. 1 particularly, shows that the V_t is 0.6292 V at V_{DS} = 0 V and the V_t drops to 0.4381V at V_{DS} = 1 V.

B. Read Stability

During correct read operation, the stored data in Q (say, storing "1") and QB (storing "0") are transferred to the bitline (BL) and bitline bar (BLB) by leaving BL at its precharged value and discharging BLB through MN3 and MN1 (Fig. 2). A careful sizing of MN1 and MN3 is needed to avoid accidental read upset due to building up of V_{QB} at QB. Minimum-sized transistors are necessary to design small-sized bitcell, which will result in longer read access time (T_{RA}) because of slow discharging of large bitline capacitance through small-sized transistor (offering higher resistance). As the difference between BL and BLB builds up, the sense amplifier (not shown) [14] is activated by asserting sense enable (SE) high to accelerate the reading process. At the point of 10% discharge of BLB, sense amplifier is enabled to sense the differential voltage between BL and BLB. Full-swing discharge of BLB does not take place. Hence, condition $V_{DS,MN3} \geq V_{GS,MN3} - V_{t,MN3}$ remains valid, which implies that NM3 remains in

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saturation region and MN1 remains in linear region. Boundary condition on MN1 and MN3 sizing to avoid read upset is achieved by equating BLB discharging currents through MN3 and MN1 as given below

$$\frac{\beta_{MN3}}{2}\left(V_{DD}-V_{QB}-V_{t,MN3}\right)^2 = \beta_{MN1}\left\{\left(V_{DD}-V_{t,MN1}\right)V_{QB}-\frac{{V_{QB}}^2}{2}\right\} \quad (3)$$

where

$$\beta = \mu_n C_{ox}\,(W/L). \quad (4)$$

Equation (3) can be solved for V_{QB} by substituting $V_{t,MN3}$ and $V_{t,MN1}$ using (2) and Table I. The Cell Ratio (CR) (also called β ratio) is defined as

$$CR = \frac{(W/L)_{MN1}}{(W/L)_{MN3}}. \quad (5)$$

CR is required to be set appropriately to avoid accidental read upset. The Fig. 3 shows the plot of V_{QB} versus CR of Dif-6T simulated using MN1/MN3 size ratio from 0.1 to 3.5 with minimum-sized transistors (i.e. MP1 = MP2 = MN2 = MN4 = 32 nm/32 nm). It is observed from Fig. 3, that the voltage rise at QB with CR = 0.1 is 0.3285 V, whereas V_{tn} ranges from 0.4381 V to 0.6292 V for V_{DS} ranging from 1 V to 0 V (Fig. 1) in 32 nm technology node. It implies that read upset may not occur due to voltage rise while reading, if CR is lowered even up to 0.1. Read stability also largely depends on DIBL, which is inherent to technology scaling (i.e. SCE). To understand the dependence of read upset on DIBL, consider the case when V_{QB} is increasing from 0. The increase in V_{QB} will increase the $V_{DS,\,MN1,}$ (Drain to source voltage of MN1). It is obvious (Fig. 1), that this will reduce the V_t of MN1 thereby making it stronger. This unexpected mismatch in threshold voltage will affect the SNM of the SRAM cell (decrease in V_t will decrease SNM) [5]. An SRAM cell should be designed such that under all conditions some SNM is reserved to cope with dynamic disturbances. Therefore, considering the trade- off between SNM and cell size, CR is set to 1 for the analysis in this paper (i.e. Dif-6T and SEP-6T cells are made with minimum-sized devices). It is therefore obvious that, neither the proposed design nor its counter part will suffer from read upset problem.

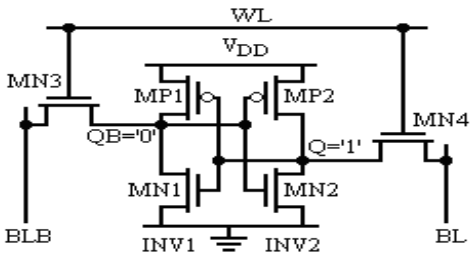

Figure 2. Standard 6T SRAM cell

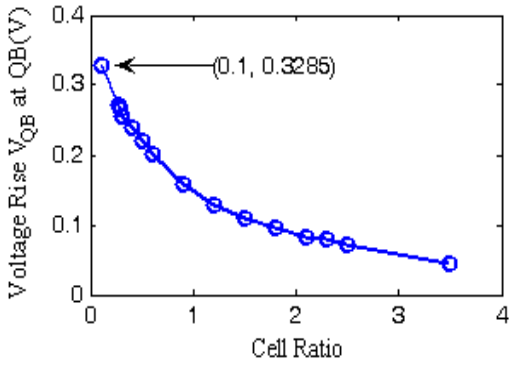

Figure 3. Voltage ripple (V_{QB}) versus cell ratio while reading Dif-6T

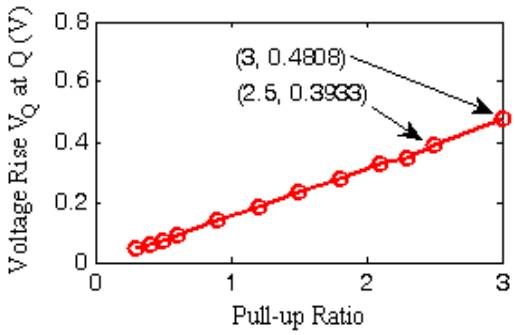

Figure 4. Voltage ripple versus pull-up ratio while writing to Dif-6T

C. *Write-Ability*

A reliable write operation is possible if node storing "1" (say, Q in Fig. 2) is pulled low enough – below the threshold voltage of MN1, so that writing a "1" is possible to the other storage node (say, QB) by flipping the cell state. Sizing of the transistors MP2 and MN4 should be such that this occurs causing flipping of state, failing which will cause write failure. The size ratio between MP2 and MN4 called pull-up ratio (PR) (also called γ ratio) is defined as

$$PR = \frac{(W/L)_{MP2}}{(W/L)_{MN4}}. \quad (6)$$

Fig. 4 plots the simulated results of V_Q versus PR with minimum-sized transistors (i.e. MP1 = MN1 = MN2 = MN3 = 32 nm/32 nm). As observed from Fig. 4, to avoid write failure, PR must be chosen such that V_Q falls below threshold voltage of MN1. As mentioned above, threshold voltage V_{tn} = 0.4381 V at V_{DS} = 1 V (Fig. 1) at 32 nm technology node. As observed from Fig. 4, V_Q = 0.4808 V at PR = 3, which implies that PR should be set below 3 to avoid write failure. The PR for the proposed design as well as Dif-6T in this paper is set to unity which ensures their write-ability.

IV. Single Ended PFET-based 6T SRAM Cell

Fig. 5 shows the proposed design. It consists of two cross-coupled inverters connected in a positive feed-back loop through transistor MP5. Unlike, conventional differential 6T SRAM cell, only one PMOS transistor MP3 is used as access transistor for accessing the cell.

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A. Read/Write operation and Cell sizing

Writing as well as reading takes place only through BLB. Thus, single ended writing and sensing (reading) scheme is required for the proposed design. All the transistors (four PMOS and two NMOS) are of minimum-sized (each 32 nm × 32 nm) to achieve smallest cell area. PMOS transistors are used as major devices to get the benefit of its higher radiation tolerance. Leakage currents in NMOS transistors increase after radiation bombardment, but leakage currents in PMOS devices remain almost unaffected [15]. Excessive leakage in access transistor may corrupt the stored data in storage node of the cell. Therefore, usage of PMOS transistors will improve the hold failure probability of the SRAM cell. Moreover, PMOS devices have an order of magnitude smaller gate leakage than NMOS transistors [16].

Before and after each write operation BLB is precharged low, by asserting PCL (pre-charge low) high at the gate of an NMOS whose drain and source are connected to BLB and GND (not shown). Write operation of SEP-6T is initiated by switching MP5 off applying W = "1" (in other time, i.e., read and hold time MP5 remains on). This breaks the feedback path and makes writing easier. In the literature single ended 5T SRAM cell is found [17], which exhibits problem while writing "1" and needs write assist method. BLB carries the complement of the bit to be stored in storage node Q (or equivalently BLB carries the bit to be stored at storage node QB). On application of WL = "0", bit applied on BLB gets complemented and stored at Q. This bit in turn drives INV1 (inverter 1) and finally a bit applied at BLB gets stored at QB. Thus, write operation involves two inverters' delay. As MP3 passes a bad "0", at the end of write "0" operation at QB, V_{Q2} is at higher potential than GND (QB). This is evident from Fig. 6, which shows various node voltages while writing "0" @ QB. Just after write operation, when W is pulled down in hold mode, MN2 may partially conduct causing short-circuit current to pass from V_{DD} to GND through MP2. This problem can be mitigated in two ways; 1) by using low-V_t (absolute value) MP5 to reduce voltage difference between Q2 and QB and 2) using high-V_t MN2 to reduce the possibility of it being on due to residual V_{Q2}. Zero bias threshold voltage (V_{tn0}) of NMOS is 0.63 V at BPTM 32 nm technology. It is already quite high compared to zero bias threshold voltage (V_{tp0}) of PMOS. Therefore, in this paper low-V_t (absolute value) MP5 is used (−0.3 V in spite of −0.5808 V). Extensive simulations are performed to obtain optimum results by selecting different V_ts. Optimum results in terms of various design metrics are obtained with the V_ts as shown in Table II. During write "0" to QB operation, BLB is precharged initially to GND but not charged. During write "1" operation at QB, BLB is initially precharged to GND and then charged by the write circuit (not shown). This reduces the switching activity factor, which helps in saving dynamic power dissipation. The write "1" to QB operation is illustrated in Fig. 7, which shows various node voltages during write operation. For the single ended read operation an inverter can be used to sense the BLB, but other single ended sensing mechanism such as charge re-distribution amplifier could improve read speed [14]. In this analysis, read operation is simulated with QB holding "1". This is illustrated in Fig. 8, which shows various node voltages while reading with QB holding "1".

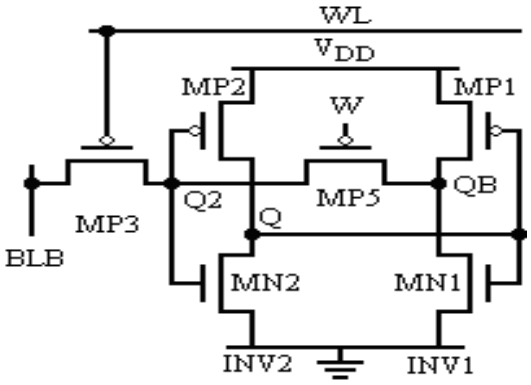

Figure 5. Proposed single ended 6T SRAM cell (SEP-6T)

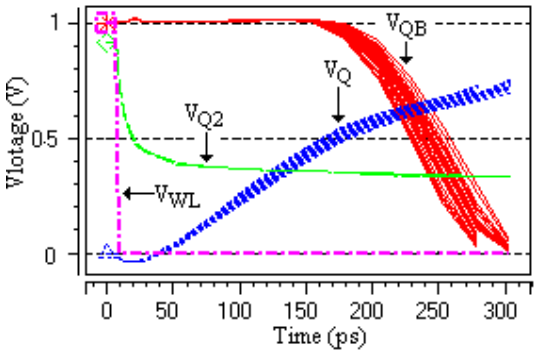

Figure 6. Voltage transfer curve (VTC) of various nodes while writing "0" @ QB

TABLE II.
THRESHOLD VOLTAGE FOR OPTIMUM RESULTS

Device	Dif- 6T	SEP-6T
MP1, MP2 V_{tp0}	−0.5808 V	−0.63 V
MP3, MP5 V_{tp0}	–	−0.30 V
MN1, MN2 V_{tn0}	0.63 V	0.63 V
MN3, MN4 V_{tn0}	0.63 V	–

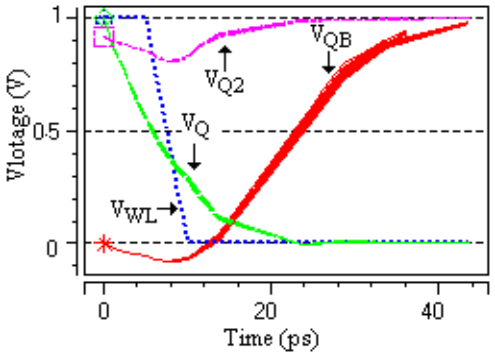

Figure 7. VTC of various nodes while writing "1" @ QB

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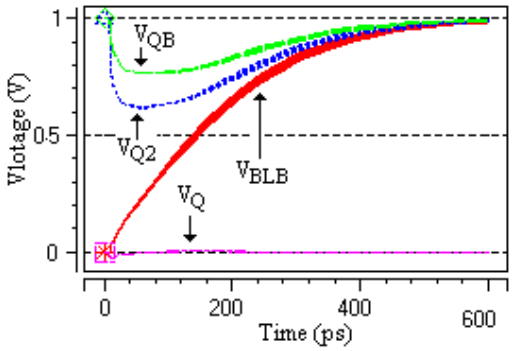

Figure 8. VTC of various nodes while reading with QB storing "1"

B. Dynamic Power Saving

The dynamic power is one of the major contributors to the total power consumption in the SRAM cell. The dynamic power consists mainly of two components – write power and read power. These power dissipations occur due to charging/discharging of large bitline capacitances. The bitline capacitance consists of source/drain diffusion capacitance of access transistor, interconnect capacitance and contact capacitance. The expression for bitline capacitance is given by

$$C_{BL} = C_{BLB} = C_{S/D,cap} + C_{\text{int}} + C_{contact}. \qquad (7)$$

The dynamic power dissipation during write operation contributes 70% to the total dynamic power dissipation in SRAM cell [18]. Write dynamic power dissipation while writing to a cell is given by

$$P_{\text{WRITE}} = \alpha_{\text{BL}} \times C_{\text{BL}} \times V_{\text{DD}}^2 \times F_{\text{WRITE}} \qquad (8)$$

where α_{BL} is the switching activity factor, F_{WRITE} is writing frequency to SRAM cell. Writing to a conventional Dif-6T cell (Fig. 2) requires discharging (from initial high value) of one of the bitlines per write operation whereas the proposed design requires charging (from initial precharged GND value) of its only bitline (BLB) while storing "1" at storage node QB (or "0" @ storage node Q). This reduces α_{BL} to ≤ 0.5. It is therefore, obvious from (8), that P_{WRITE} is improved by more than 50% if proposed design is used replacing Dif-6T.

V. Simulation Measurement Results and Discussion

This Section presents measurements of various design metrics which are measured during simulation on HSPICE using BPTM 32 nm technology [19]. Monte Carlo simulations are performed for the measurements. During Monte Carlo simulation, process parameters such as L (channel length), W (width), t_{ox}, (oxide thickness), u_0 (zero bias carrier mobility) and $R_{\square}$ (sheet resistance) are varied by ±10% with Gaussian distribution function. The temperature is varied from 24°C to 134°C as well using absolute Gaussian function. Simulation measurements are taken for both the designs applying ±3σ variation. Monte Carlo simulation is a method for iteratively evaluating a design. The goal is to determine how random PVT variations affect the performance and reliability of a design.

A. Write Access Time

Write access time (T_{WA}) is estimated at different voltages while writing "1" @ QB. Table III presents the measured T_{WA} of both the designs. Fig. 9 plots the simulated results for making the comparison easier. The T_{WA} is estimated as the time required for writing "1" at QB from the point when WL reaches 50% of its full swing from its initial high level to the point when QB rises to 90% of its full swing from its initial low level. As mentioned in Section IV-A, for writing a bit @ QB, the write operation is completed after a two inverter delays when QB settles to its new state. Therefore, the T_{WA} is longer than T_{RA} (read access time) as shown in Section V-D. To understand why the T_{WA} of SEP-6T is lower than that of Dif-6T, remember that, V_t of MP2 ($V_{tp0} = -0.5808$ V) of Dif-6T is lower (absolute value) than that of MP2 ($V_{tp0} = -0.63$ V) of SEP-6T, Thus, MP2 of Dif-6T is stronger than that of SEP-6T. This prevents MN4 of Dif-6T to drop V_Q quickly. Another reason of lower write delay in SEP-6T is that the MP3 ($V_{tp0} = -0.3$ V) of SEP-6T passes a strong "1" from BLB to drive INV2 (inverter 2) harder and MP2 of SEP-6T is also made weaker by increasing its V_t (absolute value). This helps MN2 to quickly pull down storage node Q, which in turn drives INV1 and quickly flips QB. As observed from the Table III, proposed design offers 29.7% improvement in T_{WA} at nominal voltage of $V_{DD} = 1$ V.

TABLE III.
Write Access Time

SRAM	T_{WA} while writing "1" @ QB (s)	V_{DD} (V)
Dif-6T	3.853e-11	1
	4.751e-11	0.95
	5.467e-11	0.90
	6.542e-11	0.85
	8.047e-11	0.80
SEP-6T	2.709e-11	1.00
	3.163e-11	0.95
	3.962e-11	0.90
	5.741e-11	0.85
	7.794e-11	0.80

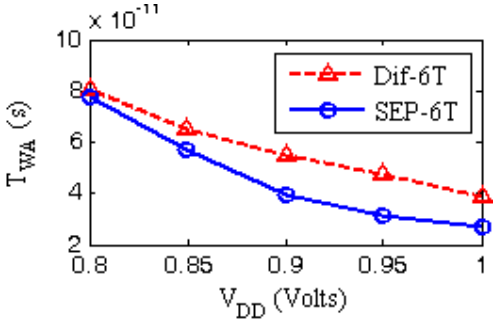

Figure 9. Write access time while writing "1" QB

B. Write Power Measurement

Write dynamic power defined in (8) is caused due to charging/discharging of bitline. Dynamic power dissipation

during accessing a cell through its devices is generally ignored, though it contributes a large portion to the total dynamic power consumption. During write access in SEP-6T, while writing "1" at QB, V_{DD} finds path to GND through two pull-down transistors MN1 and MN2 (Fig. 5). BLB is asserted high for writing "1" @ QB. BLB is connected to Q2 through MP3 while writing. The supply at BLB does not find path to GND. Therefore, major dynamic power dissipation during transition (accessing) is through MN1 and MN2. Thus, total average write transition power of SEP-6T is given by

$$P_{W,SEP-6T} = P_{AVG,MN1} + P_{AVG,MN2} \quad (9)$$

where $P_{AVG,MN1}$ and $P_{AVG,MN2}$ are average write transition power through MN1 and MN2 while writing "1" @ QB. In case of Dif-6T, BLB is biased at V_{DD} and BL is grounded by write circuit (not shown). BL pulls-down storage node Q below switching threshold of INV1 and finally flips the cell to write a "1" @ QB. During this transition, V_{DD} finds path to GND through three transistors MN1, MN2 and MN4. Therefore, total average write transition power of Dif-6T is given by:

$$P_{W,Dif-6T} = P_{AVG,MN1} + P_{AVG,MN2} + P_{AVG,MN4} \quad (10)$$

where $P_{AVG,MN1}$, $P_{AVG,MN2}$ and $P_{AVG,MN4}$ are average write transition power through MN1, MN2 and MN4 while writing "1" @ QB. Total average write transition power, i.e., $P_{W,SEP-6T}$ and $P_{W,Dif-6T}$, commonly abbreviated as W_{PWR} is estimated at different voltages while writing "1" @ QB and the results are plotted in Fig. 10, which shows that the SEP-6T outperforms Dif-6T at all supply voltages. Equations (9), (10) and the above discussion clarify the reason of its superiority. As observed from the Fig. 10, proposed design offers 38.5% improvement in W_{PWR} at nominal voltage of V_{DD} = 1 V.

C. Write EDP Measurements

Reduction of EDP is a good direction for optimizing any digital circuit including SRAM cell. Since EDP reflects the battery consumption (E) for completing a job in a certain time (D), it is an important design metrics. Therefore, EDP of SEP-6T and Dif-6T are estimated and results are compared. The write energy delay product (W_{EDP}) is estimated using write delay and write power while writing "1" @ QB. The W_{EDP} of SEP-6T is defined as

$$W_{EDP,SEP-6T} = P_{W,SEP-6T} \times T^2_{WA,SEP-6T}. \quad (11)$$

The W_{EDP} of Dif-6T is defined as

$$W_{EDP,Dif-6T} = P_{W,Dif-6T} \times T^2_{WA,Dif-6T}. \quad (12)$$

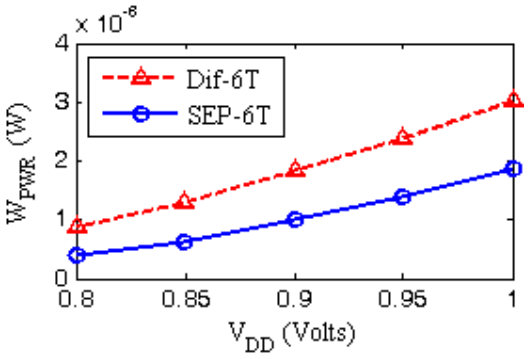

Figure 10. Total average write transition power versus V_{DD}

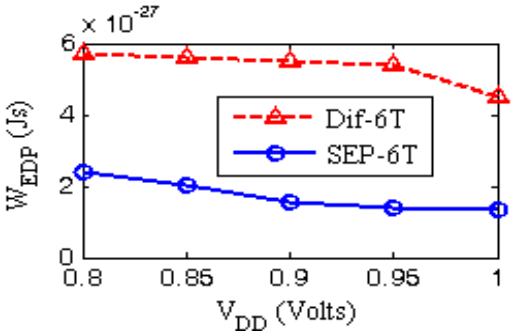

Figure 11. Write EDP (W_{EDP}) estimated at different voltages while writing "1" @ QB versus V_{DD}

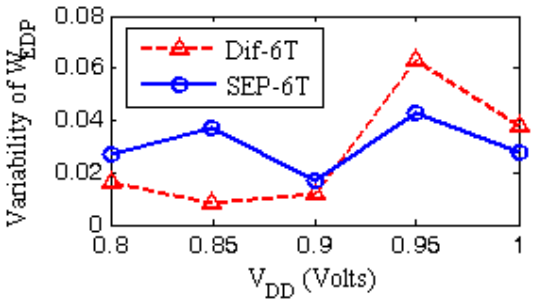

Figure 12. Write EDP (W_{EDP}) variability estimated at different voltages while writing "1" @ QB versus V_{DD}

The measurements of W_{EDP} are taken at various operating voltages starting from nominal voltage of V_{DD} = 1 V down to the minimal operating voltage of 0.8 V beyond which write failure begins to occur under the used writing condition (if write condition is changed write failure may not occur). The results are plotted in Fig. 11, which shows that the SEP-6T outperforms Dif-6T at all supply voltages. As observed from the Fig. 11, proposed design particularly offers 69.6% improvement in W_{EDP} at nominal voltage of V_{DD} = 1 V.

Write EDP (W_{EDP}) variability (σ/μ) is estimated at various supply voltages and the results are plotted in Fig. 12. As observed from Fig. 12, fluctuations in W_{EDP} of Dif-6T at lower voltages are quite satisfactory, but it shoots up at 0.95 V, whereas variations in SEP-6T are moderate at all supply voltages. To make both the circuits variation immune in terms of W_{EDP}, they are to be operated at 0.9 V. As observed from the Fig. 12, proposed design offers

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26.3% improvement in W_{EDP} variability at nominal voltage of V_{DD} = 1 V.

D. Read Access Time

As mentioned in Section IV-A, for single ended read operation an inverter can be used to sense the BLB, but other single ended sensing mechanism could decrease the read delay. Read access time (T_{RA}) is estimated at different voltages with QB storing "1" for both the design at iso-measuring condition (i.e., with equal WL slew rate, on time and same operating voltage). The measured results are reported in Table IV. The results are also plotted in Fig. 13 for making comparison easier.

The T_{RA} (for Dif-6T) is estimated as the time required for reading with QB storing "1" from the point when WL reaches 50% of its full swing from its initial low level to the point when BL falls by 10% of its full swing from its initial high level. The T_{RA} (for SEP-6T) is estimated as the time required for reading with QB storing "1" from the point when WL reaches 50% of its full swing from its initial high level to the point when BLB rises to 90% (so that inverter connected to BLB to sense its voltage is able to do so without fail) of its full swing from its initial low level. As observed from Fig. 13, SEP-6T outperforms Dif-6T at all supply voltages except at nominal voltage of V_{DD} = 1 V (where T_{RA} of SEP-6T equals T_{RA} of Dif-6T).

TABLE IV.
READ ACCESS TIME

SRAM	T_{RA} with QB storing "1" (s)	V_{DD} (V)
Dif-6T	1.667e-11	1
	1.913e-11	0.95
	2.255e-11	0.90
	2.764e-11	0.85
	3.574e-11	0.80
	5.040e-11	0.75
SEP-6T	1.644e-11	1
	1.790e-11	0.95
	1.984e-11	0.90
	2.242e-11	0.85
	2.588e-11	0.80
	3.028e-11	0.75

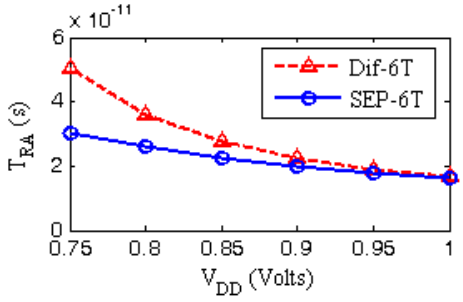

Figure 13. Read access time while writing "1" QB

To understand why the T_{RA} of SEP-6T is lower than that of Dif-6T, remember that, large C_{BL} discharges (while reading with QB holding "1") through high-V_t MN4 (V_{tn0} = 0.63 V) of Dif-6T whereas in case of SEP-6T, C_{BLB} is charged through low-V_t MP3 (V_{tp0} = − 0. 3 V). It implies that MN4 does not get on till 0.63 V is applied at its gate through WL, whereas only |0.3 V| applied through WL is sufficient to put MP3 on. Since slew rate of WL is same for both the cases C_{BLB} begins to charge up earlier than C_{BL} begins to discharge down.

E. Read Power Measurement

Read power is measured with QB holding "1". During read access in SEP-6T, V_{DD} finds path to GND through two pull-down transistors MN1 and MN2 and storage node holding "1" charges C_{BLB} through MP5 and MP3 (Fig. 5). Therefore, total average read transition power of SEP-6T is given by

$$P_{R,SEP-6T} = P_{R\_AVG,MN1} + P_{R\_AVG,MN2} + P_{BLB} \quad (13)$$

where $P_{R\_AVG,MN1}$ and $P_{R\_AVG,MN2}$ are average read transition power through MN1 and MN2 and P_{BLB} is power dissipated for charging C_{BLB} while reading with QB storing "1". The P_{BLB} per read operation is given by

$$P_{BLB} = C_{BLB} \times V_{DD}^2 \times f_t \quad (14)$$

where f_t is transition or read frequency. In case of Dif-6T, BL and BLB are biased at V_{DD} before each read operation. During read transition V_{DD} finds path to GND through MN1 and MN2. C_{BL} discharges through MN2 via storage node Q. Therefore, total average read transition power of Dif-6T is given by

$$P_{R,Dif-6T} = P_{R\_AVG,MN1} + P_{R\_AVG,MN2} \quad (15)$$

where $P_{R\_AVG,MN1}$ and $P_{R\_AVG,MN2}$ are average read transition power through MN1 and MN2 while reading with QB storing "1".

Total average read transition power, i.e., P_{R_SEP-6T} and P_{R_Dif-6T}, commonly abbreviated as R_{PWR} is estimated at different voltages while reading with QB storing "1" and the results are plotted in Fig. 14. As observed from Fig. 14, the proposed design outperforms the conventional Dif-6T at all higher supply voltages staring from 0.85 V

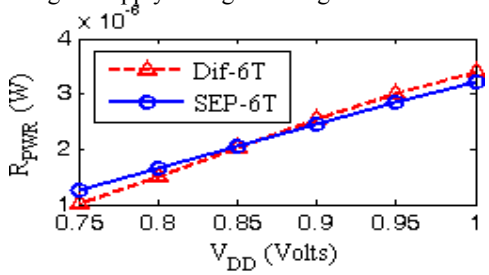

Figure 14. Total average read transition power (R_{PWR}) estimated at different voltages while reading with QB storing "1" versus V_{DD}

to nominal voltage of 1 V. At lower voltages such as 0.75 V and 0.8 V, Dif-6T outperforms SEP-6T. As observed from the Fig. 14, proposed design offers 5.6% improvement in R_{PWR} at nominal voltage of V_{DD} = 1 V.

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F. Read EDP Measurements

The Read Energy Delay Product (R_{EDP}) of SEP-6T and Dif-6T are estimated and results are compared. R_{EDP} is estimated using read delay and read power while reading with QB holding "1". The R_{EDP} of SEP-6T is defined as

$$R_{EDP,SEP-6T} = P_{R,SEP-6T} \times T^2_{RA,SEP-6T} \quad (16)$$

The R_{EDP} of Dif-6T is defined as

$$R_{EDP,Dif-6T} = P_{R,Dif-6T} \times T^2_{RA,Dif-6T} \quad (17)$$

The measurements of R_{EDP} are taken at various supply voltages starting from nominal voltage of V_{DD} = 1 V down to the minimal supply voltage of V_{DD} = 0.75 V beyond which read failure begins to occur under the used reading condition (if read condition is changed read failure may not occur). The results are plotted in Fig. 15. As observed from Fig. 15, SEP-6T outperforms Dif-6T at all supply voltages.

G. Static Noise Margin Measurements

The SNM of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. SNM of an SRAM is a widely-used design metric that measures the cell stability. Fig. 16 and 17 show conceptual test setup for measuring SNM for SEP-6T and Dif-6T respectively. The measured results when plotted is called "butterfly curve". Fig. 18 plots the combined "butterfly curve" of Dif-6T and proposed SEP-6T at iso-measuring condition. The butterfly curve for SEP-T is obtained in the following way using the test circuit: 1) W and BLB are biased at GND voltage and WL is biased at supply voltage. 2) Voltage of N1 is swept from 0 V to supply voltage while measuring voltage of QB. 3) Voltage of N2 is swept from 0 V to supply voltage while measuring voltage of Q in the same way. 4) Measured voltages are plotted to get butterfly curves. The side length of Maximum Square that can be embedded within the smaller lobe of the butterfly curve represents the SNM of the cell. This definition holds good because, when the value of noise voltage (V_{N1} or V_{N2}) increases from 0, the VTC (voltage transfer characteristic) for INV1 formed with MP1 and MN1 moves to the right and the VTC^{-1} (inverse VTC) for INV2 formed with MP2 and MN2 moves downward. Once they both move by the SNM value, the curves meet at only two points and any further noise flips the cell [20]. As observed from Fig. 18, SEP-T shows 22.5% penalty in SNM.

H. Comparitive Study of Cell Area

In multi-port design, area would be the major concern. As multi-core µPs, SoCs, and NoCs (network-on-Chip)

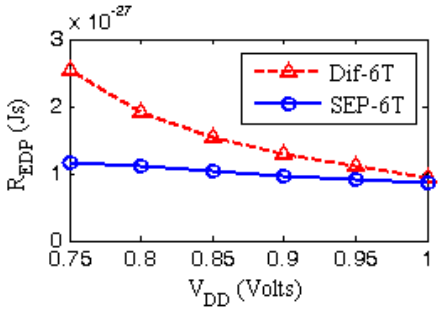

Figure 15. Read EDP versus V_{DD}

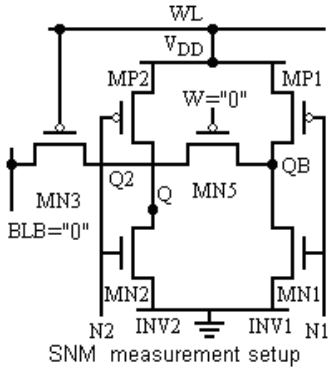

Figure 16. Test circuit for measurement of SNM of SEP-6T

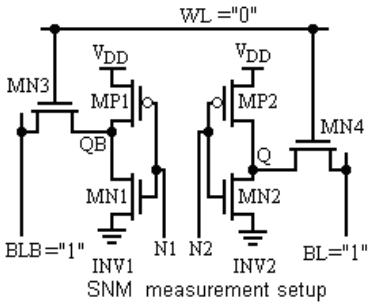

Figure 17. Test circuit for measurement of SNM of Dif-6T

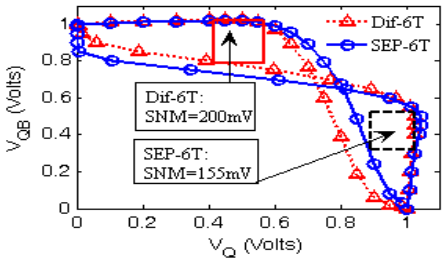

Figure 18. Static noise margin of Dif-6T and proposed SEP-6T cell

will dominate future technological innovation, on-chip cache deigned with high density and low bitline switching power is an attractive choice. In 65 nm technology node, RD-8T (read decoupled 8T) SRAM cell proposed in [21], isolates read port from storage node thereby increasing read stability (without improving write margin significantly) at cost of 30% area penalty compared to dense 6T cell (which might me used for higher level caches). Differential data-aware power-supplied D^2AP 8T cell with a boosted bitline scheme proposed in [22], incurs an area overhead similar to

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RD-8T cell. This design also slightly degrades hold static noise margin (SNM) due to stacking effect. Authors in [23] proposed a 10T SRAM cell which solves column interleaving problem without any extra access delay but at the expense of large area penalty. A 32-bit word with single-ended 6T SRAM bitcell in [24] consumes 16% (including the read and write assist transistors) larger area than standard 6T bitcell and 14% less than 8T proposed in [25]. In view of area constraint in future on-chip-cache, this paper proposes a novel single-end 6T SRAM cell that consumes less area on chip compared to standard Dif-6T considering the layout of bitline routing.

VI. Conclusion

This paper presents a PFET-based single ended 6T SRAM cell which is radiation hardened and capable of saving write dynamic power. It has successfully demonstrated that the proposed design is robust against the impact of process, voltage and temperature variations in terms of tighter spread in write EDP. The simulation measurement results confirm the successful functionality and read/write stability of the proposed design. The benefits of read and write power reduction make it an attractive choice for applications where static noise is negligible.

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